Design and Development of GPS Receiver for PNSS-1

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Overview

• Introduction
• Various implementations of GPS receivers
• Proposed design
• Results
• Conclusion
Global Positioning System is a satellite based navigation system made up of a network of 24 satellites

- Developed by US DoD
- Early on, humans used stars to navigate
**GPS Receiver**

Block Diagram of GPS Receiver
Design Challenges

- Accuracy
- Cost
- Flexibility
FPGA Based GPS Receivers

• Main processing module is designed on FPGA
  • Real-time GPS receiver implemented on Altera FPGA Board [1]

• Soft-cores based implementations are also available
  • FPGA and Micro-Blaze based GPS receiver [2]
**DSP Based GPS Receivers**

- A GPS L1 Software Receiver Implementation on a DSP Platform [3]
- Implementation of a Complete GPS receiver on the C6713 DSP [4]
- Simulation and Analysis of GPS Software Receiver [5]
GPS Receiver for PNSS-1

• We are presenting GPS receiver for Pakistan National Students Satellite One

• Can be used in any other micro satellite

• The role of the GPS receiver is to provide orbital position and velocity of PNSS-1
Implementation

GPS Receiver has 4 main modules

Block Diagram
**RF Front End**

- RF front end module consists of
  - Antenna
  - Frequency down converter
    - Low Noise Amplifier (LNA)
    - Band Pass Filter (BPF)
    - Frequency Mixer
  - Analog to Digital converter
Acquisition Module

- Satellite signals are interpreted only if
  
i. Local carrier matches the carrier of the incoming signal
  
ii. Local *Pseudo Random Noise (PRN)* codes are well aligned in time with the PRN of the incoming signal
In tracking loops, the incoming signals are followed by two types of loops namely Frequency Lock Loop (FLL) and/or Phase Lock Loop (PLL).
Navigation

• Demodulation takes place at this stage of the correlated values generated in the previous stages

• Kalman filter is applied in the end to calculate the pseudo range.
Working

- The antenna receives the signal and forwards it to the front-end module.
- The front-end module preprocesses the data, converts it to the digital domain, and passes the digital signal to the main processing unit.
- The processing unit calculates the position information and passes it to the On-Board Computer (OBC) through the CAN interface.
- The OBC sends the information to the ground station.
Results

- The intended design satisfies the requirement of the PNSS-1
- These are
  - Positional accuracy better than 20m
  - Update rate greater than 1 Hz
Thank you for your attention!
References

1. Yerabati, S.; Zhen Hu; Elkeelany, O., "Real-time GPS receiver implemented using Altera FPGA Board," IEEE SoutheastCon 2010 (SoutheastCon), March 2010


